Amendments to the Claims:

Please amend Claim 1. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing:

1. (currently amended) A multiplier circuit comprising:

a frequency generating circuit which generates an output signal at a rate that is a multiple of input frequency of an input signal;

a phase comparator which directly compares the phase of an edge of the input signal with the phase of an edge of the output signal and controls the frequency generating circuit based on the comparison.

2. (original) A multiplier circuit as claimed in claim 1 further comprising a window signal applied to the phase comparator, the window signal being true during edges of the input signal and output signal to be compared.

3. (original) A multiplier as claimed in claim 2 further comprising a divider which frequency divides the output signal to provide the window signal.

4. (original) A multiplier circuit as claimed in claim 3 wherein the frequency generating circuit is a voltage-controlled oscillator.

5. (original) A multiplier circuit as claimed in claim 1 wherein the frequency generating circuit is a voltage-controlled oscillator.

6. (original) A method of frequency multiplying comprising:

generating an output signal at a rate that is a multiple of an input signal; and

directly comparing the phase of an edge of the input signal with the phase of an edge of the output signal and controlling the frequency of the output signal based on the comparison.

7. (original) The method as claimed in claim 6 further comprising applying a window signal to a phase comparator which compares the phase.

8. (original) A method as claimed in claim 7 further comprising dividing the output signal to provide the window signal.

9. (original) A method as claimed in claim 8 wherein the output signal is generated in a voltage controlled oscillator.

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10. (original) A method as claimed in claim 6 wherein the output signal is generated in a voltage controlled oscillator.

11. (previously presented) A method as claimed in Claim 6 wherein the phase of the edge of the input signal is directly compared with the phase of the edge of the output signal in combinational circuitry having an output which depends only on the state of an input to the combinational circuitry.

12. (previously presented) A method as claimed in Claim 6 wherein the phase comparator produces up and down pulses which, when the phase of the edge of the input signal is aligned with the phase of the edge of the output signal, each have a duration which is a fraction of the input signal and the output signal transition times.

13. (previously presented) A method as claimed in Claim 6 wherein the phase of the edge of the input signal is directly compared with the phase of the edge of the output signal by applying the input signal and output signal to gates of transistors which are coupled in a combinational logic circuit.

14. (previously presented) A method as claimed in Claim 13 wherein the combinational logic circuit provides current source and drain to an output as up and down current pulses.

15. (previously presented) A multiplier circuit as claimed in Claim 1 wherein the phase of the edge of the input signal is directly compared with the phase of the edge of the output signal in combinational circuitry having an output which depends only on the state of an input to the combinational circuitry.

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16. (previously presented) A multiplier circuit as claimed in Claim 1 wherein the phase comparator produces up and down pulses which, when the phase of the edge of the input signal is aligned with the phase of the edge of the output signal, each have a duration which is a fraction of the input signal and the output signal transition times.

17. (previously presented) A multiplier circuit as claimed in Claim 1 wherein the phase of the edge of the input signal is directly compared with the phase of the edge of the output signal by applying the input signal and output signal to gates of transistors which are coupled in a combinational logic circuit.

18. (previously presented) A multiplier circuit as claimed in Claim 17 wherein the combinational logic circuit provides current source and drain to an output as up and down current pulses